REMARKS

The Examiner is respectfully thanked for the thoughtful consideration provided to this application. Reconsideration of this application is respectfully requested in light of the foregoing amendments and the following remarks.

Claim 7 was amended solely for purposes of addressing informalities, and thus, not for reasons related to patentability.

Claims 4 – 11 are now pending in this application. Each of claims 4, 5, 7, 9, and 11 are in independent form.

The Indefiniteness Rejections

Claim 7 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is respectfully traversed. Claim 7 has been amended solely for addressing informalities.

Thus, reconsideration and withdrawal of this rejection is respectfully requested.

The Obviousness Rejections

Each of claims 4-11 was rejected under 35 U.S.C. 103(a) as being unpatentable over various combinations of Moran (U.S. Patent No. 5,519,843) in view of Stripf (U.S. Patent No. 6,263,487). These rejections are respectfully traversed.

Filed herewith is a 37 CFR § 1.132 Declaration of Dr. Ronald D. Williams, a professor of engineering at University of Virginia, and one skilled in the art of electrical engineering.

None of the cited references, either alone or in any combination, establish a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to

combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *See* MPEP 2143.

Examination Note

As an initial matter, the rejection of claim 9 in the present Office Action indicates that an Agrawal reference is used as a basis for claim rejection. See pages 8-9. Applicant presumes that this rejection refers to Agrawal (U.S. Patent No. 5,179,716), but can find no support at locations recited in the present Office Action in Agrawal for any of the elements alleged to be present therein. Applicant will respectfully treat recitations to Agrawal as recitations to Moran.

Moran Uses Three Chips

Each of independent claims 4, 5, 7, 9, and 11 recite "**a single chip** program execution device" "**lacking a memory device external to said single chip** program execution device."

Paragraphs 11-18 of Dr. Williams' Declaration provide evidence that one skilled in the art would not find that Moran expressly or inherently teaches or recites "**a single chip** program execution device" "**lacking a memory device external to said single chip** program execution device." Stripf does not overcome the deficiencies of Moran.

Thus, even if there were motivation or suggestion to modify or combine the cited references (an assumption with which the applicant disagrees), and even if there were a reasonable expectation of success in combining or modify the cited references (another assumption with which the applicant disagrees), the cited references still do not expressly or inherently teach or suggest **every** limitation of the independent claims, and consequently fail to establish a *prima facie* case of obviousness.

Because no *prima facie* rejection of any independent claim has been presented, no *prima facie* rejection of any dependent claim can be properly asserted. Consequently, reconsideration and withdrawal of these rejections is respectfully requested.

Apparent Official Notice

To the extent that Official Notice is taken to support the rejection, Applicants respectfully traverse and request citation and provision of a reference that supports the rejection. *See* MPEP 2144.03.

Specifically, each of independent claims 4, 5, 7, 9, and 11 recite a "**programmable logic controller**." The present Office Action recites "Moran discloses a **programmable controller** (Fig. 9)." See Page 3. The present Office Action further recites "an integrated controller (see Fig. 9) and the use of code to emulate more than one type of devices (see col.7, lines 14-23) wherein a programmable memory stores user programs for effecting logic to implement the control over an OS and related functionalities as taught by Moran (see SUMMARY) suggests a form of programmable logic controller, and the concept of emulation/simulation of multiple devices requiring control is suggested." See Page 4. Paragraphs 19-26 of Dr. Williams' Declaration provide evidence that one skilled in the art would not find that Moran expressly or inherently teaches or recites a "programmable logic controller."

Apparent Inherency

Moran fails to properly establish inherent anticipation of claim elements claimed in the present Office Action. *See* MPEP 2112. "Inherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." Trintec Indus., Inc. v. Top-U.S.A. Corp., 295 F.3d 1292, 1295, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002). No evidence has been presented that the admittedly "missing descriptive material is 'necessarily present'" in Moran. For example, the present Office Action recites:

1. "[n]or does Moran explicitly teach that the programmable controller is being implemented for executing a compilation is to implement PLC I/O functions and that the compilation comprises system support kernel. But in view of Moran's teachings as to be able to initialize the power settings or memory input/output resetting of the controller (e.g. col.3, lines 16 to col. 5, line 35; Fig. 7), such kernel related support instructions as well as input/output routines or I/O functions are strongly **implied** if not disclosed. See Page 4; and
2. "[n]or does Moran explicitly specify a single chip program execution device separable for a communication/programming device; but in view of the teachings of user code being flashed into a single device for emulating a hard drive of the device (see Fig. 9; col. 6, line 59 to col. 7, line 3), this limitation is disclosed." See Page 5;
3. "[n]or does Moran explicitly disclose compiling to form said binary programmable logic control program; however, Moran teach no source code for being loaded in memory for execution, only user program being loaded to support the BIOS system functionality of the controller (col. 7, line 59 to col. 7, line 3). Hence this compiling limitation is **implicitly** disclosed." See pages 6-7;

Applicant respectfully requests evidence demonstrating that the admitted "missing descriptive material is 'necessarily present'" in Moran.

Moran Does Not Teach or Suggest Programmable Logic Controller I/O functions

Independent claim 4 recites ""programmable logic controller I/O functions." Paragraphs 27-32 of Dr. Williams' Declaration provides evidence that one skilled in the art would not find that Moran expressly or inherently teaches or recites """"programmable logic controller I/O functions." Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 4.

Placing a Single Chip Program Execution Device in Stripf Would Render Stripf Inoperative

It is inappropriate to combine references when the combination produces a seemingly inoperative device. See, Nat's Steel Car, Ltd. v. Canadian Pac. Ry., Ltd., 357 F.3d 1319, 1339 (Fed. Cir. 2004); Tec Air Inc. v. Denso Mfg. Mich. Inc., 192 F.3d 1353, 1360 (Fed. Cir. 1999) (quoting In re Sponnoble, 405 F.2d 578, 587 (CCPA 1969).

Paragraphs 33-38 of Dr. Williams' Declaration provides evidence that one skilled in the art would find combining elements alleged to be present in Moran with Stripf would render at least Stripf inoperative for its intended purpose.

Thus, even if Moran disclosed claim limitations asserted in the present Office Action, a premise that Applicant disputes, attempting to combine Moran with Stripf would cause Stripf's programmable logic controller to cease functioning according to the "**requirements**" disclosed therein. Thus, one skilled in the art would find no motivation or suggestion to modify or combine the cited references. With or without Stripf, Moran fails to establish a *prima facie* obviousness rejection

Because no *prima facie* rejection of any independent claim has been presented, no *prima facie* rejection of any dependent claim can be properly asserted. Consequently, reconsideration and withdrawal of these rejections is respectfully requested.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

> "none of the references of record alone or in combination disclose or suggest the combination of limitations found in the independent claims. Namely,
>
> - claim 4 is allowable because none of the references of record alone or in combination disclose or suggest 'a single chip program execution device' 'a

single chip program execution device comprising: a micro controller operable to implement programmable logic controller I/O functions upon executing a compilation comprising the user program and a system support kernel, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program; and a re-programmable read only memory within which the compilation is stored, said single chip program execution device separable from a communication/programming device adapted to convert the user program to a binary code module and combine the binary code module with the system support kernel into a single executable firmware module, said programmable logic controller lacking a memory device external to said single chip program execution device';

- claims 5 and 6 are allowable because none of the references of record alone or in combination disclose or suggest 'receiving a symbolic user program at a communication/programming device, said communication/programming device separable from a single chip program execution device having a re-programmable read only memory, said single chip program execution device adapted to execute a binary programmable logic control program, said binary programmable logic control program stored within said re-programmable memory, said binary programmable logic control program adapted to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and compiling, at said communication/programming device, said symbolic user program to a binary code module; and combining the binary code module with a system support kernel to form said binary programmable logic control

program, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program';

- claims 7 and 8 are allowable because none of the references of record alone or in combination disclose or suggest 'receiving, from a communication/programming device, a binary programmable logic control program at a single chip program execution device having a re-programmable read only memory, said communication/programming device separable from said single chip program execution device, said binary programmable logic control program comprising a compilation of a symbolic user program combined with a system support kernel to form a single executable module, the system support kernel adapted to provide a programmable logic controller with operating system functions comprising sequencing the user program, said single chip program execution device adapted to execute said binary programmable logic control program to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and loading said binary programmable logic control program into said re-programmable read only memory of said program single chip execution device';

- claims 9 and 10 are allowable because none of the references of record alone or in combination disclose or suggest 'within a single chip, a program execution device having a re-programmable memory, said program execution device adapted to execute a binary programmable logic control program, said binary programmable logic control program stored within said re-programmable

memory, said binary programmable logic control program comprising a compilation of a user program and a system support kernel, said binary programmable logic control program adapted to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and a communication/programming device separable from said program execution device, said communication/programming device providing functions required for external communication of said binary programmable logic control program, said binary programmable logic control program comprising a binary module formed from compiling a symbolic user program, the binary module combined with a system support kernel to form a single executable module, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program, said communication/programming device adapted to load said binary programmable logic control program into said re-programmable memory and wherein said binary programmable logic control program is stored in said re-programmable memory of said program execution device by direct manipulation of logic controls of said re-programmable memory'; and

- claim 11 is allowable because none of the references of record alone or in combination disclose or suggest 'receiving a symbolic user program at a communication/programming device, said communication/programming device separable from a single chip program execution device having a re-programmable read only memory, said single chip program execution device adapted to execute a binary programmable logic control program, said binary programmable logic control program stored within said re-programmable

memory, said binary programmable logic control program adapted to operate a programmable logic controller, said binary programmable logic control program comprising a binary module derived via compiling a symbolic user program, the binary module combined with a system support kernel to form a single executable module, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program, said programmable logic controller lacking a memory device external to said single chip program execution device; and compiling, at said communication/programming device, said symbolic user program with a system support kernel to form said binary programmable logic control program".

PATENT

Application # 09/697,419

Attorney Docket # 1999P07938US01 (1009-045)

CONCLUSION

It is respectfully submitted that, in view of the foregoing amendments and remarks, the application as amended is in clear condition for allowance. Reconsideration, withdrawal of all grounds of rejection, and issuance of a Notice of Allowance are earnestly solicited.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. 1.16 or 1.17 to Deposit Account No. 50-2504. The Examiner is invited to contact the undersigned at 434-972-9988 to discuss any matter regarding this application.

Respectfully submitted,

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Date: 2 May 2005

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